AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A bus arbiter coupled to a first and second bus master, a first and second slave and a bus, comprising:

at least one port coupled to receive bus request commands for a transaction from either the first or second bus master and coupled to receive an address or identity of the first and second slaves for the transaction, and also coupled to communicate over the bus; and

logic circuitry that defines logic to select a bus frequency according to the requested transaction.

2. (Original) The bus arbiter of claim 1 wherein the logic circuitry defines logic to select a bus frequency according to the identity of the slave for the requested transaction.

3. (Original) The bus arbiter of claim 1 wherein the logic circuitry defines logic to select a bus frequency according to the identity of the master for the requested transaction.

4. (Original) The bus arbiter of claim 1 wherein the logic circuitry defines logic to select a bus frequency according to the length of the bus between the first or second master and the first or second slave according to which ones are involved in the requested transaction.

5. (Previously Presented) A method for generating sample cycle pulses, comprising:

determining a ratio of an internal clock of a device to the clock of a bus; and

generating a sample cycle pulse in an appropriate cycle of the internal [[or]] clock with respect to the ratio.

6. (Previously Presented) The method of claim 5 wherein the ratio of clocks is determined by counting the negative or falling edges of the faster clock pulses in two periods of the slower clock and dividing by 2.

Claims 7-9 (Cancelled)

10. (Previously Presented) A method for selecting a bus frequency, comprising:

setting a bus frequency according to a transaction having a source and a destination

the bus frequency being such that a device receiving a communication of the transaction will have a frequency that is an integer multiple of the bus frequency.

11. (Previously Presented) The method of claim 10 further comprising determining the identity of a master bus and its corresponding internal frequency.

12. (Previously Presented) The method of claim 10 further comprising determining the identity and corresponding internal frequency of a slave or receiver device.

13. (Previously Presented) The method of claim 10 further comprising determining the identity of the devices in the transaction and examining a table to determine a corresponding bus frequency.

14. (Original) The method of claim 10 wherein the bus frequency for the transaction is determined dynamically rather than by performing a table lookup.

15. (Original) The method of claim 10 wherein the bus frequency also is set according to an expected or determined amount of impedance in the bus between the terminals that are a part of the transaction.

16. (Original) The method of claim 10 wherein the bus frequency is determined by a bus arbiter.

17. (Original) The method of claim 10 wherein the bus frequency is determined by a clock generation controller.

18. (Original) The method of claim 10 wherein the frequency of the bus is determined by a bus master.

19. (Previously Presented) A bus slave, comprising:

at least one input port for receiving communication signals and control signals;

circuitry for determining a bus frequency;

circuitry for determining a ratio between an internal clock of the bus slave and the bus frequency; and

circuitry for determining when to latch a communication signal being received over the at least one input port with respect to the ratio.

20. (Previously Presented) The bus slave of claim 19 further including a state machine for generating a sample cycle signal, the sample cycle signal prompting the bus slave to latch the communication signals as a part of determining when to latch the communication signal.

21. (Previously Presented) A system, comprising:

first and second bus masters;

first and second slaves;

a bus coupled to the first and second bus masters and the first and second slaves; and

a bus arbiter coupled to the bus, the bus arbiter comprising:

at least one port coupled to receive bus request commands for a transaction from either the first or second bus master and coupled to receive an address or identity of the first and second slaves for the transaction, and also coupled

to communicate over the bus; and

logic circuitry that defines logic to select a bus frequency according to the requested transaction.

22. (Original) The system of Claim 21, wherein the logic circuitry defines logic to select a bus frequency according to the identity of the slave for the requested transaction.

23. (Original) The system of Claim 21, wherein the logic circuitry defines logic to select a bus frequency according to the identity of the master for the requested transaction.

24. (Original) The system of Claim 21, wherein the logic circuitry defines logic to select a bus frequency according to the length of the bus between the first or second master and the first or second slave according to which ones are involved in the requested transaction.

25. (Original) The system of Claim 21, wherein the bus arbiter is processor-based.

26. (Original) The system of Claim 21, wherein the bus arbiter comprises one of a group of technologies consisting of: application-specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), and FPGAs that include embedded core processors and embedded ASIC circuitry.

27. (Original) The system of Claim 26, wherein the bus arbiter includes dedicated hardware logic that performs table lookup and arbitration tasks.

28. (Original) The system of Claim 21, wherein the first slave comprises:

at least one input port for receiving communication signals and control signals from the bus;

circuitry for determining a bus frequency;

circuitry for determining a ratio between an internal clock of the bus slave and the bus frequency; and

circuitry for determining when to latch communication signals being received over the at least one input port.

29. (Original) The system of Claim 28, wherein:

the circuitry for determining when to latch communication signals includes a state machine; and

the state machine generates a sample cycle signal that prompts the slave to latch the communication signals.

Claims 30-34. (Cancelled)